Cont'd B3

or pressure welding, and another face is connected to another power terminal of said two power terminals by soldering or pressure welding.

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1-19 are pending in the present application with Claims 1 and 11 having been amended by the present amendment.

In the outstanding Office Action, Claims 1-4, 6-8, 10-13, 15-17 and 19 were rejected under 35 U.S.C. § 102(b) as anticipated by Matsuda; Claims 5, 14 and 19 were rejected under 35 U.S.C. § 103(a) as unpatentable over Matsuda; and Claims 9 and 18 were rejected under 35 U.S.C. § 103(a) as unpatentable over Matsuda.

Claims 1-4, 6-8, 10-13, 15-17 and 19 stand rejected under 35 U.S.C. § 102(b) as anticipated by Matsuda. This rejection is respectfully traversed.

Amended Claim 1 is directed to a semiconductor device including at least three power terminals provided one above another, and at least one semiconductor chip having a top surface and a bottom surface and interposed between two power terminals of the at least three power terminals in a direction intersecting the top surface and the bottom surface, with the top and bottom surfaces electrically connected thereto, respectively. Independent Claim 11 includes similar features.

In a non-limited example, Figures 1A and 1B illustrate a semiconductor device including at least three power terminals 3, 8, 4, provided one above another, and at least one semiconductor chip 11 having a top surface and a bottom surface and being interposed between a predetermined two power terminals (e.g., in Figure 1B between power terminals 3

and 8) in a direction intersecting the top surface and the bottom surface with the top and bottom surfaces of the semiconductor chip 11 electrically connected to the two power terminals 3 and 8.

The outstanding Office Action states Matsuda teaches the claimed invention. However, Applicants note the semiconductor chip (transistor 29 and diode 31) has top and bottom surfaces arranged in an up-and-down direction (i.e., vertical direction), whereas the three power terminals 3, 5, 7 are arranged in a direction perpendicular to the up-and-down direction (i.e., the three terminals are arranged in a horizontal direction). This is opposite to the claimed invention in which the direction of a line extending through the top surface and the bottom surface of the semiconductor chip coincides with the direction of a line extending through the two power terminals.

Accordingly, it is respectfully submitted that independent Claims 1 and 11 and each of the claims depending therefrom patentably define over Matsuda et al.

Further, regarding the additional rejections noted in the outstanding Office Action, it is respectfully requested these also be withdrawn as the claims rejected therein are dependent claims.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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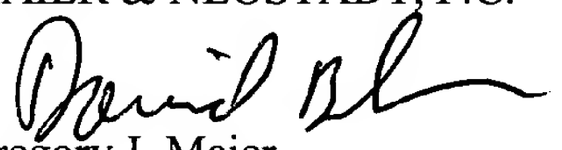
MAIER & NEUSTADT, P.C.



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IN THE SPECIFICATION

Please amend the specification as follows:[3]

Page 1, please replace the paragraph beginning at line 21 to page 2, line 7 as follows:

In FIG. 9A, a collector side of an IGBT chip 65 and an n layer side of a diode chip 66 are soldered respectively, on a Cu pattern 63 of the surface of a DBC (Direct Bond Copper) substrate wherein copper conductors sandwich an insulation substrate 67 of alumina. An emitter side of the IGBT chip 65 and a p layer side of the diode chip 66 are connected with an external power terminal 61, through an Al bonding wire of, for example, 200 to 500 μmφ, extending from both chips. On the other hand, the surface Cu pattern 63 is connected to an external power terminal 62. Such structure is [place] placed on a heat radiation plate 69. In FIG. 9A, a gate terminal 70 shown in FIG. 9B is not illustrated.

IN THE CLAIMS

--1. (Twice Amended) A semiconductor device comprising:

at least three power terminals provided one above the other; and

at least one semiconductor chip having [an upper] a top surface and a [lower] bottom surface and interposed between a predetermined two power terminals of said at least three power terminals in a direction intersecting the top surface and the bottom surface, with the

[3]A marked-up copy of the change made to the specification is attached.

[upper] top and [lower] bottom surfaces of the at least one semiconductor chip electrically connected to the two power terminals.

11. (Amended) A semiconductor device comprising:

at least three power terminals provided one above another; and

at least one semiconductor chip having [an upper] a top surface and a [lower] bottom surface and interposed between a predetermined two power terminals of said at least three power terminals in a direction intersecting the top surface and the bottom surface, with the [upper] top and [lower] bottom surfaces of the at least one semiconductor chip electrically connected to the two power terminals,

wherein one face of said at least one semiconductor chip interposed between said two power terminals is connected to one power terminal of said two power terminals by soldering or pressure welding, and another face is connected to another power terminal of said two power terminals by soldering or pressure welding.--